

TID and SEE Response of Advanced Samsung and Micron 4G NAND Flash Memories for the NASA MMS Mission

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Abstract— SEE and TID results are presented for two advanced commercial flash memories, Samsung and Micron 4Gb. Both have very good TID response, and very good SEU bit error rates, but the Samsung parts have lower SEFI rates and lower rates of destructive failures.

I. INTRODUCTION

This study was undertaken to determine and compare the susceptibilities of 4 Gbit NAND Flash memories from Samsung and Micron to destructive and nondestructive single-event effects (SEE) and to TID (Total Ionizing Dose) damage for the NASA MMS (Magnetosphere Multi-Scale) mission. The devices were monitored for SEUs, errors from individual cells, for SEFIs, errors arising in the control logic, and for destructive events, including latchup, induced by exposing them to a heavy ion beam at the Texas A&M University Cyclotron.

II. DEVICES TESTED

We tested a total of four Micron parts, out of eight available (part number MT29F4G08AAAWP, Lot Date Code (LDC) 748) in the SEE test, plus nine more in the TID test. For the Samsung SEE tests, we used a total of 23 parts, from five different date codes (part number K9F4G08U0A-PCB0, LDCs 840, 843, 846, 901, and 907). The Samsung TID test used five more parts from each of these LDCs. For both manufacturers, the parts have 512Mx8 organization with large blocks. That is, the blocks are 128Kx8, with 64 pages/block. Each page is nominally 2Kx8, but they also have 64 redundant columns, which makes the total page size 2112x8. NAND flash normally has some bad blocks which can be screened off. The specification is that no more than 80 of the 4096 blocks

will be bad. In our experience, the parts almost always have a few bad blocks, but it is usually a single digit number. Note that with commercial devices, the same LDC does not guarantee that the parts are from the same manufacturing facility.

The device technology is 63 nm minimum feature size CMOS NAND Flash memory. All the parts are single die, SLC (single level cells). The chips came in a 48-pin TSOP package, but the plastic had been dissolved on the topside to expose the chips, allowing the beam to reach the chip surface.

III. TEST METHODS AND CONDITIONS

Because Flash technology uses different voltages and circuitry depending on the operation being performed, testing was performed for a variety of test patterns and bias and operating conditions, using the NASA LCDT (low Cost Digital Tester), shown in Fig. 1.

Test patterns included all 0's, all 1's, checkerboard and inverse checkerboard. In general, all zeroes is the worst-case condition for single bit errors. For a zero, the floating gate is fully charged with electrons. An ion can have the effect of introducing positive charge, which may be enough to cause a zero-to-one error. However, a checkerboard pattern (AA) was used in most of the testing because errors in the control circuitry can cause errors of both polarities. One-to-zero errors are an indication that the errors are coming from the control circuits. Between exposures, all patterns can be used to exercise the DUT, to verify that it was still fully functional. However, all patterns are not used on every shot, just because it is time consuming to do so. The maximum clock frequency for these devices was 40 MHz, which is also the frequency used in the dynamic testing.

Bias and operating conditions included:

- 1) Static/Unbiased irradiation, in which a pattern was written and verified, and then bias was removed from the part and the part was irradiated. Once the irradiation reached the desired fluence, it was stopped, bias was restored, and the memory contents were read and errors tallied.
- 2) Static irradiation, which was similar to unbiased irradiation, except that bias was maintained throughout irradiation of the part.

Note that these conditions provide no opportunity to

This work was supported in part by the NASA' MMS Program and NASA Electronic Parts and Packaging Program (NEPP).

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monitor functional or hard failures that may occur during the irradiation.

- 3) Dynamic Read, in which a pattern was written to memory and verified, then subsequently read continuously during irradiation. This condition allows determination of functional, configuration and hard errors, as well as bit errors. In this mode, the number of static bit errors is determined by reading the memory again, after the beam is turned off.
- 4) Dynamic Read/Write, which was similar to the Dynamic Read, except that a write operation is performed on each word found to be in error during the previous Read.
- 5) Dynamic Read/Erase/Write, which again was similar to the Dynamic Read and Read/Write, except that a word in error was first erased and then rewritten. In this mode, the words that are read are compared to an "expected" pattern, which is actually the complement of the stored pattern. For this reason, every word is erased, as if it were in error. Because the Erase and Write operations use the charge pump, it is expected that the Flash could be more vulnerable to destructive conditions during these operations.
- 6) Latchup (SEL) testing was conducted at 70° C, and 3.6 V. There were no cases where SEL was observed, but there were other destructive failures at high temperature. Therefore, we did extensive testing in the range 40-70°C at 3.3 V, although we did not consider it to be SEL testing. The goal of this high temperature testing was to detect destructive events, other than SEL.
- 7) In this set of experiments, we have attempted to look at angular effects, which may include multiple bits grazed by the same ion, and other effects due to charge sharing by multiple nodes in the control logic. This test was done with at 45 degrees, which was close to the maximum possible angle, because the socket would have blocked the beam at angles much higher. There were two orientations, which we referred to as 45° North, and 45° East. Although the normal bit error upset rate is somewhat higher at high angles, probably because of charge sharing in the control logic, destructive failures occur primarily at normal incidence. For this reason, much of the high temperature testing was done at normal incidence.

TID testing was done at a Co-60 facility, which is a room air source, where the Co-60 rods are raised up out of the floor, during exposures. Active dosimetry is performed, using air ionization probes. Testing is done in a step/stress manner, using a standard Pb/Al filter box. Dose rate typically varies slightly from one exposure to the next, up to 12 rads/s. The

source no longer delivers the dose rate called for by MIL-STD Test Method 1019.7, but it is still well above the dose rate encountered in a space environment. Time intervals for testing between exposures are within the limits stated in 1019.7 (one hour after exposure to start electrical characterization, two hours to begin the next exposure). Parts were under DC bias during exposures, but not actively exercised.

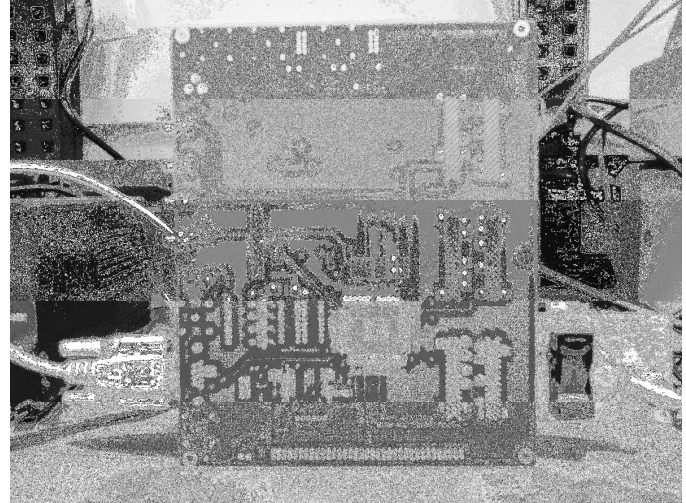


Fig. 1. LCDT Test System

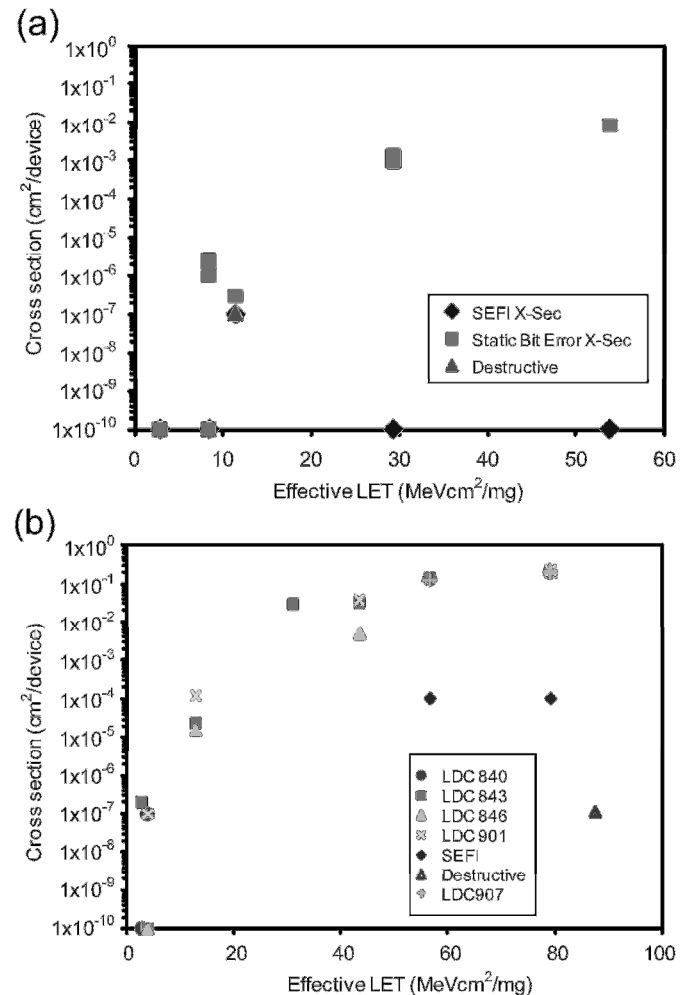


Fig. 2. Unbiased static results: (a) Micron; (b) Samsung

SEE testing was done at the Texas A&M Cyclotron, using the 15 MeV/ nucleon tune, using the ions given in Table I:

TABLE I: IONS/ENERGIES AND LET FOR THIS TEST.

TAMU Ions	Energy/ AMU	Energy (MeV)	Approx. LET on die (MeV•cm ² /mg)	Angle	Effective LET
Ne	15	300	2.8	0, 45	2.8, 3.9
Ar	15	600	8.4	0, 45	8.4, 11.8
Kr	15	1260	30.1	0, 45	30.1, 41
Xe	15	1965	54.8	0, 45	54.8, 75
Au	15	2955	87.5	0	87.5

IV. RESULTS

During testing, the DUTs were irradiated with the ions indicated in Table I. The DUT was oriented normal to the incident beam, or at 45 degrees. The errors observed in static SEU testing are shown in Fig. 2, with no bias applied. The 45 degree data is plotted at the effective LET (LET/cos θ). This is done so that one can distinguish between the normal incidence shots and the 45 degree shots. It is not done because effective LET is expected to be a useful concept for other reasons.

In the unbiased static mode, for the Micron parts, there were two exposures at 45° incidence with Ar ions (LET=8.4), which produced two SEFIs and one destructive failure of the erase circuit. We did not have enough samples to destroy them at that rate, especially at such low LET, so we concentrated on getting normal incidence results. We intended to return to high angle exposures later, but ran out of beam time before we could do so. For the Samsung parts, many more exposures were required, because five different LDCs had to be tested separately. In all, there were 27 shots in this test mode for the Samsung parts. Fourteen of these were at high angle. There was only one destructive failure, with Au ions at normal incidence—that is, at LET about an order of magnitude higher than for the Micron destructive failure. The results for both manufacturers are summarized in Fig. 3.

In the static mode with bias, for the Micron parts, there were 36 SEFIs due to block errors (where an entire block of 128Kx8 bits was lost, presumably due to a single ion), plus four other SEFIs, one of which was a destructive latchup (SEL). For the Samsung parts, there were a total of 27 shots, with 18 shots at oblique angles, with three SEFIs and no destructive failures. These results are summarized in Fig. 3.

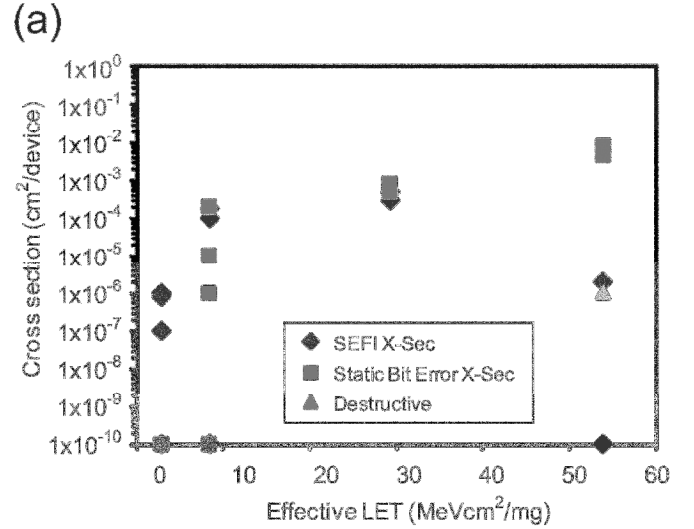


Fig. 3a. SEU, SEFI, and destructive failure results for Micron parts, in static mode with bias.

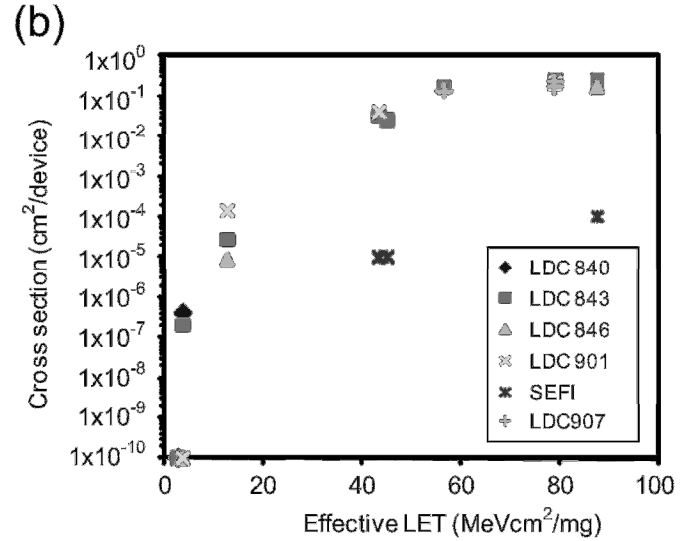


Fig 3b. Samsung results for SEU, SEFI, and destructive failures, in static mode with bias.

For the Dynamic Read mode, results are shown in Fig. 4, for both manufacturers. Here, and also in the other dynamic test modes, transient errors are defined as those observed while the part is operating with the beam on. Static errors are the bits in error after the beam is turned off. For the Micron parts, there were a total of ten shots, with 36 block errors and two other SEFIs, with no destructive events. For the Samsung parts, there were 24 shots, including 17 at high angles, with two SEFIs and no destructive events.

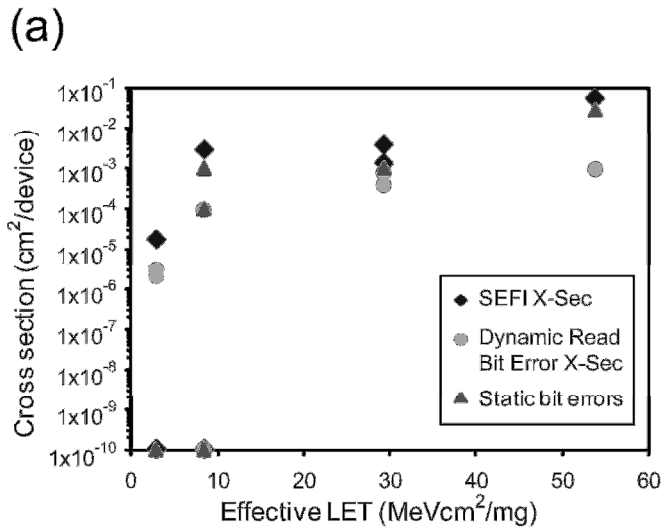


Fig. 4a. Micron dynamic read mode results for SEU, SEFI, and destructive failures.

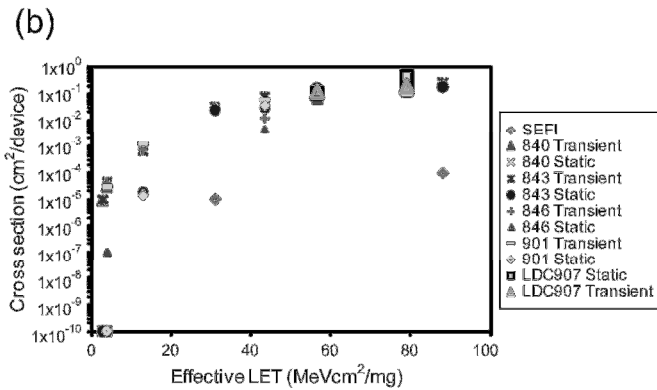


Fig 4b. Samsung dynamic read mode results for SEU, SEFI, and destructive failures.

Results for the Dynamic R/W mode, for both manufacturers, are shown in Fig 5. For the Micron parts, there were ten shots in this test mode, there were 48 block errors and one other SEFI, and no destructive events. For the Samsung parts, there were 32 shots, including 24 at high angle, and nine at high temperature, with eight SEFIs and two destructive events. These were an erase failure with Au ions and a write failure with Xe ions.

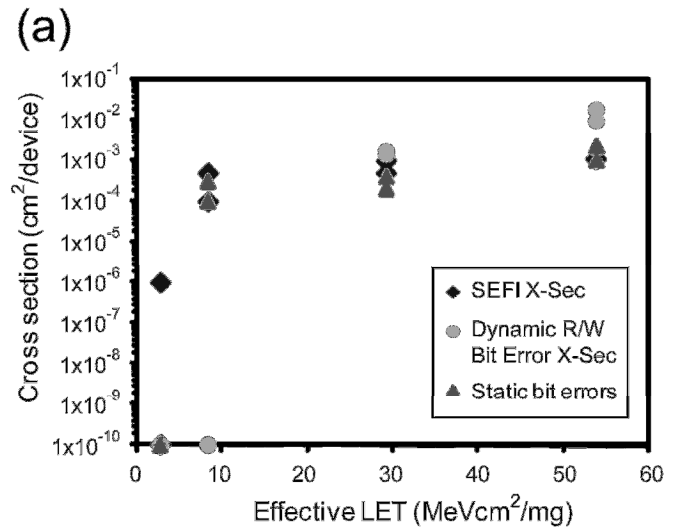


Fig 5a. Micron dynamic R/W mode results for SEU, SEFI, and destructive failures.

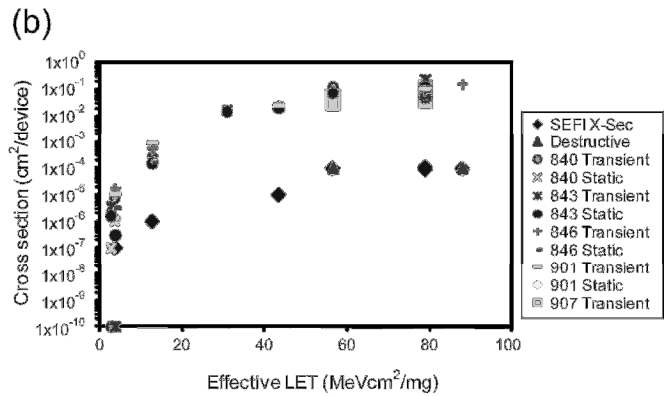


Fig 5b. Samsung dynamic R/W mode results for SEU, SEFI, and destructive failures.

Results for the Dynamic R/E/W test mode are shown in Fig. 6 for both manufacturers. In this mode, the high voltage erase and write operations are both being performed, so it was expected that this would be the worst case test condition for failures related to those operations. For the Micron parts, there were 15 shots, with 33 block errors and one other SEFI, plus one destructive latchup (SEL). For the Samsung parts, there were 77 shots in this mode, including 46 at high angle, and 54 at elevated temperature. In the first test trip, we found that the Samsung parts failed at high temperature (70° C) more often than at room temperature. Therefore, we made a second test trip to examine this temperature sensitivity in more detail. The Micron parts, on the other hand, failed at all temperatures, so we did not pay special attention to their high temperature response. The Samsung parts had 24 SEFIs and nine destructive events. These destructive events occurred only at normal incidence, even though most shots were at high angle. They occurred mostly (six of the nine events) at high temperature, and with high LET ions (eight of the nine with Xe or Au ions). The high temperature results for the Samsung parts for all the test modes are summarized in Table II.

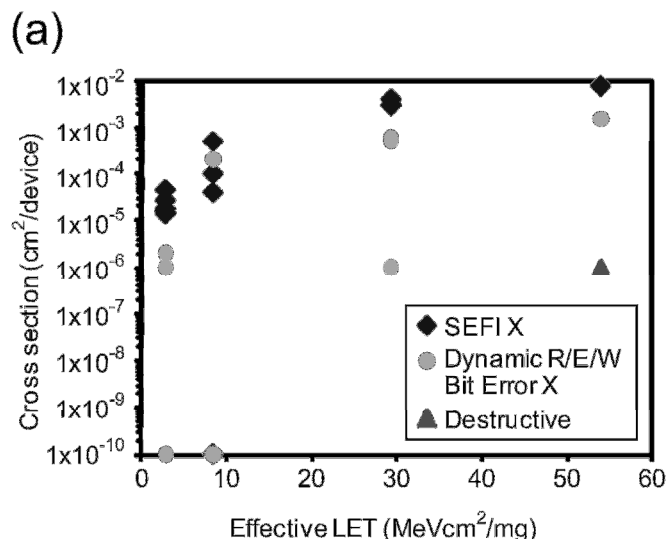


Fig 6a. Micron results in dynamic R/E/W mode for SEU, SEFI, and destructive failures.

Summarizing the results of these tests: all the high T failures were with Xe ions (LET=56), none were observed with Kr (next lowest LET=31). Because there were no failures with Kr, no testing was done with other, lower LET ions. All the high temperature failures were at normal incidence—there was not a single failure at high angles. All the failures occurred in either the R/E/W test mode or the R/W mode—there were no failures if the high voltage erase and write operations were not being performed. Summarizing the results in Table II by LDC:

- 1) LDC 840 had four parts that failed in either the R/E/W or R/W test modes. Two failed on the first 70° C shot at normal incidence, in the first test run. Two more failed at room temperature and normal incidence in second test.
- 2) LDC 843, there were two erase failures at room temperature and normal incidence in the first test. One was with Au ions in the Dynamic Read mode, and the other was in R/E/W mode with Ar ions. In the second test, there was one additional failure, with Xe ions at high temperature. This sample failed on the first high temperature shot at normal incidence, at 40° C, but it had survived 11 other shots at higher angles, at temperatures over the range 40-70° C. This part had a write mode failure, but it was unlike the other write mode failures. In most cases, when the write circuit failed, it failed completely, and every address in the entire memory was bad. For this part, however, the write circuit worked for all but 159 addresses (stuck bits), even though it was drawing 53 mA, compared to 15-16 mA, nominal write current. This was an incomplete write, not a complete failure.
- 3) LDC 846 had one write failure at normal incidence and room temperature with Au ions in the first test. One other sample failed in the second test at

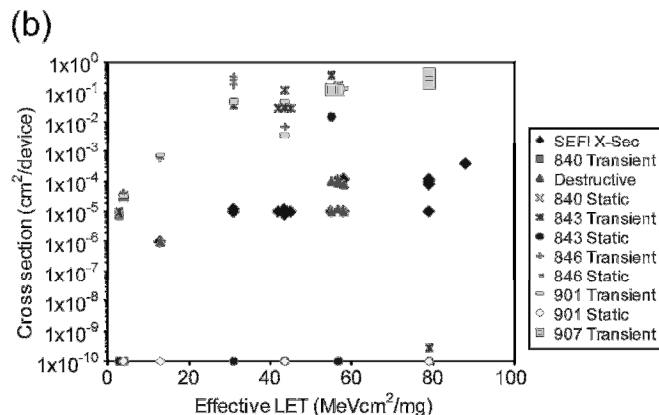


Fig 6b. Samsung results in dynamic R/E/W mode for SEU, SEFI, and destructive failure.

normal incidence and 40° C, with Xe ions. This part had survived three previous shots at 45° incidence, and 40-70° C.

- 4) LDC 901 had a write failure with Au ions at normal incidence and room temperature, and another write failure with Xe ions (normal incidence, 70° C) in the first test. In the second test, there was one additional failure, at normal incidence and 70° C. However, the sample had survived four previous shots at 45° incidence, 40-70° C, and also four shots at normal incidence, over the same temperature range. This sample had survived one shot at 70° C and normal incidence, with fluence of 10^4 particles/cm², but it failed on a second shot under these conditions, when the fluence was increased to 10^5 particles/cm².
- 5) LDC 907 had only one sample tested, because of what we believe was corrosion on the leads of several others, which made them unusable. This one sample was exposed for no less than 31 shots, all with Xe, and 15 of them at elevated temperature. It survived twelve shots at 45° incidence, 40-70° C. It also survived two normal incidence shots at 40° C, before failing at 50° C. The write current had risen on this part, from the normal 15-16 mA, to above 25 mA, before the normal incidence shots began. For this reason, we expected it to fail, before it actually did, as a result of cumulative damage. Damage on the shot where failure actually occurred was only a small part of the story, for this part.

TABLE II. SUMMARY OF SAMPLES USED AND FAILURE MODES.

LDC	Sample No.	No. Shots	Ion	Fluence (p/cm ²)	Angle (degrees)	T (° C)	Comments
840-Test trip 1	2	1	Au	9e6	0	25	Unbiased static, erase failure
	3	10	Ne	1e7	0	25	1 SEFI, still functional
	3	1	Xe	1e5	0	70	R/E/W – write fail
	4	1	Xe	1e4	0	70	R/E/W – write fail
840-Test trip 2	B7	10	Xe	1e4/shot	5 @0, 5@45	25	Write fail in R/W mode, normal inc.
	B6	1	Xr	1e4	0	25	Write fail, R/E/W
843-Test trip 1	1	3	Au	1.2E5 total	0	25	Erase fail – Dyn. Read
	2	10	Ne	1e7/shot	5@0, 5@45	25	1 SEFI, but still functional
	7	10	Xe	1e4/shot	5@0, 5@45	25	1 SEFI, but still functional
	3	10	Kr	1e5/shot	5@0, 5@45	25	1 SEFI, but still functional
	4	5	Ar	1e6/shot	5@45	25	Erase fail – R/E/W
843-Test trip 2	20	12	Xe	1e4/shot	11@45E, 1 normal	40-70 40	Normal inc. fail from stuck bits (incomplete write) – R/E/W
	22	6	Kr	1e5/shot	2@45E, 4@0	40-70 40-70	1 SEFI, but still functional
846-Test trip 1	4	2	Au	1e4/shot	0	25	R/W – write fail
	7	5	Ne	1e7/shot	45	25	No SEFIs, fully functional
		5	Xe	1e4/shot	45	25	No SEFIs, fully functional
		6	Kr	1e5/shot	45	25	3SEFIs, fully functional
		5	Ar	1e6/shot	45	25	No SEFIs, fully functional
846-Test trip 2	B10	4	Xe	1e4/shot	3 @ 45, 1 @ 0	40-70 40	Write fail at normal inc., R/E/W
	B12	12	Kr	1e5/shot	4 @ 45, 4 @ 0	40-70 40-70	4 total SEFIs, but fully functional
901-Test trip 1	1	2	Au	3.5e4 total	0	25	Write fail – R/E/W
	3	5	Ne	1e7/shot	45	25	No SEFIs, fully functional
		5	Xe	1e4/shot	45	25	No SEFIs, fully functional
		1	Xe	1e5	45	70	SEFI, functional after PC
	4	1	Xe	1e5	0	70	Write fail
	6	5	Kr	1e5/shot	45	25	No SEFIs, fully functional
		5	Ar	1e6/shot	45	25	No SEFIs, fully functional
901-Test trip 2	B04	9	Xe	1e4/shot	4 @ 45, 5 @ 0	40-70 40-70	Write fail at normal inc., 70 C R/E/W
	B03	7	Kr	1e5/shot	3 @ 45, 4 @ 0	40-70 40-70	2 SEFIs, fully functional
907-Test trip 2	13	6	Xe	1e4/shot	0	25	No SEFI, fully functional
		10	Xe	1e4/shot	45	25	No SEFIs, fully functional
		6	Xe	2.4e5 total	45	70	1 SEFI, fully functional
		6	Xe	1e4/shot	45	2 ea. @ 40, 50, 60	1 SEFI, fully functional
		3	Xe	1e4/shot	0	2 @ 40, 1 @ 50	Write fail @ 50, R/E/W Write current high before normal inc. shots

The power supply current was monitored on all shots, and representative sample traces are shown in Figs. 7-11. Typical power supply current traces are shown in Figs. 7 and 8 for two exposures using Xe ions in the R/E/W test mode. Fig 7 is at 25° C, and neither a permanent failure, nor a SEFI occurred. Fig. 8 is at 70° C, and both a SEFI and a permanent write

failure occurred. For these parts, normal read current is about 10-11 mA., and write current in a fresh part is about 15-17 mA, although it increases as a part degrades over multiple shots. Erase current is 8-9 mA, and the current is about 4 mA, when the part is idling, not doing anything. In Fig. 7, the sample starts to read, and then the beam is turned on, and write

pulses start, as errors are found. Write pulses continue after the beam is off, until all the errors are corrected, but the part continues to read after that, just to make sure. Finally, there is another read to verify the part is ready for the next shot. Fig. 8 shows the sample starting to read, then to have write pulses as errors begin to occur, but then the current increases to 20, 30, 40, 50 mA, and higher. When the beam is off, current stabilizes at about 57 mA. The write circuit had failed—the bit map showed the entire memory erased, because the erase circuit still worked, but none of the rewrite operations were successful. Fig. 9 shows the power supply current for a static (with bias) shot, where no SEFI occurred. The sample idles at 4 mA while the beam is on. After the beam is off, there is a read operation to count errors, and a second read to check for annealing, then an erase to prepare for the next shot, a read to verify the erase, a write to restore the test pattern and a final read to verify the write. Fig. 10 shows a similar power supply current trace, for a Dynamic read mode shot. The sample reads while the beam is on, then there is another read to count static errors after the beam is off, followed by an erase, a read to verify the erase, a write, and another read to verify the part is ready for the next shot. Fig. 11 shows results for a R/W mode shot. The sample writes while the beam is on, then reads static errors (twice), then erases, reads, writes, and reads again to verify the part is ready for the next shot. Note that in none of these current traces do we see the current spikes that have been reported elsewhere [1].

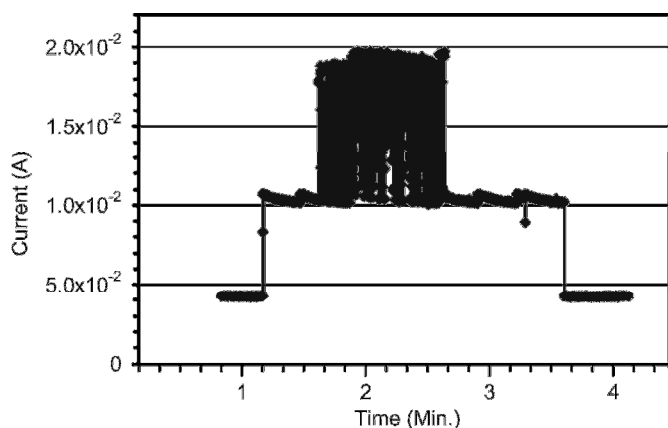


Fig. 7. Power supply current in R/E/W mode, Xe ions, at 25° C, with no permanent failure.

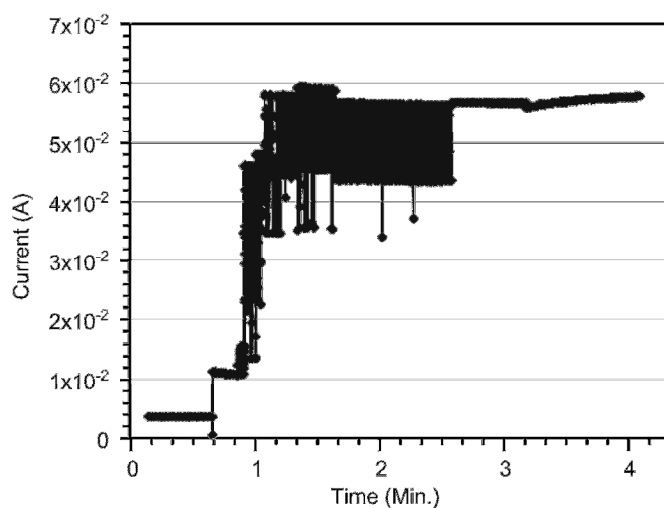


Fig. 8. Power supply current in R/E/W mode, Xe ions, at 70° C, with permanent write mode failure.

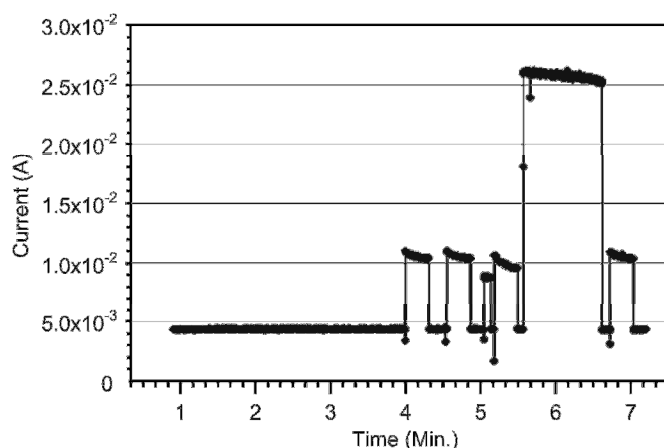


Fig. 9. Power supply current in Static mode, with bias, Ar ions, with no failure.

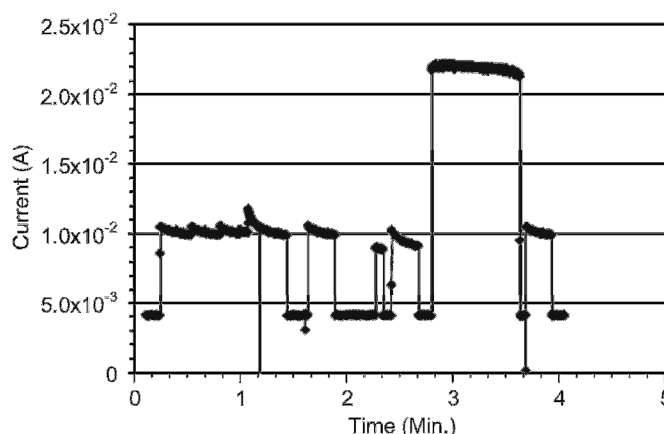


Fig. 10. Power supply current in Dynamic Read mode, Kr ions, with no failure.

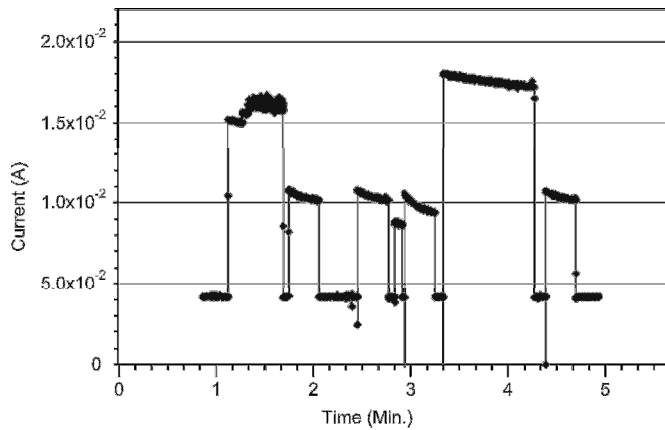


Fig. 11. Power supply current in R/W mode, Xe ions, with no failure.

Both the Micron and Samsung parts had very good TID response. The first failure, of nine Micron parts tested, occurred between 160 and 170 krad (SiO₂). The other eight parts were still functional at 200 krad (SiO₂), when the test was stopped, because the equipment had to be shipped for the SEE tests. For the Samsung parts, there was some variation between LDCs, but no part failed at less than 150 krad (SiO₂). For the most recent LDC, 907, the parts all passed at 200 krad (SiO₂), and failed at 225 krad (SiO₂).

V. DISCUSSION

In the first test run for the Samsung parts, we had three destructive write mode failures at normal incidence, and 70° C, with Xe ions. We estimated it took about 52,000 particles/cm², to produce these failures. In the second, follow-up test, only one sample (LDC 901, sample B04) was tested at 70° C and normal incidence. All the others failed at lower temperature, before we could get to 70° C. This one sample survived one shot with fluence 10⁴ particles/cm², and failed part way through another exposure to 10⁵ particles/cm². If we estimate the total fluence to failure at 3x10⁴ particles/cm², then we have four total failures with a mean fluence between failures a little over 2x10⁴ particles/cm². In geosynchronous orbit, the flux at the LET of Xe ions is about one particle/cm² per 125 years, which means there would be one chip failure per 2.5 million chip years. However, this flux is integrated over 4π steradians, and the angular test results clearly show that failures happen only when the incident particle is aligned just right. This failure interval has to be multiplied by 4π, to account for the angular dependence. These failures also occur only in the high voltage operations, Program and Erase, which are estimated to have about a 2% duty cycle—certainly less than 5%. If these correction factors are applied, the interval between failures is estimated to be more than 600 million chip-years, in geosynchronous orbit. Other orbits would generally be even longer. For a system with 2000 chips, the system failure rate would be one failure per 3x10⁵ years. If we include the three parts that failed at lower temperatures, they survived about 4x10⁴ particles/cm before the failures occurred. The totals would then be seven failures in about 1.2x10⁵ particles/cm², or about 1.7x10⁴ particles/cm² between failures.

That is, the estimated interval between failures is reduced by only about 15%. We note that many more shots were taken at room temperature, and also at the next lowest LET (Kr) at temperature, and similar failures were not observed, so there is a sensitivity at high temperature (and only at high temperature), with high enough LET, that had not been noted before. There were occasional destructive failures at room temperature, but these were failures of the erase circuit, and not the write circuit, with one exception. The one room temperature write failure happened when there was a watchdog error, meaning that the DUT stopped responding to all commands. After cycling power, we found that the write circuit did not work, any longer. We did not observe the current increase described above, which was characteristic of the other failures, at high temperature.

To estimate the error rate expected in space, given the cross sections in Figs. 2-6, we did one CRÈME96 run for geosynchronous orbit, using the following Weibull parameters: threshold LET=2.8, Width =37, exponent = 5, and saturation cross section = 7.5e-11 μm²/bit. This curve bounds all five of the measured cross sections, with some margin in all cases. The result was a bit error rate of 6.35x10⁻¹² errors/bit-day, which is approximately five orders of magnitude better than a typical volatile memory. For a 4G memory, this is equivalent to 0.025 errors/chip-day, or about 50 bit-errors per day for a system with 2000 chips. Handling this error rate should be well within the capabilities of error-correcting software. SEFIs are more difficult to correct, but, as Figs. 2-6 show, the cross section is typically 3-4 orders of magnitude less than the bit error cross section, even on shots where SEFIs occur. However, most shots have no SEFIs, so the average cross-section is really much lower than the Figures indicate. Based only on the cross-sections in Figs. 2-6, the system SEFI rate, assuming 2000 chips, is estimated to be .005-.05 events/day, or one event every 20-200 days. Based on all shots, the rate is perhaps an order of magnitude lower. Most of these can be corrected by cycling power, and reprogramming the corrupted portion of the memory, so the impact to the mission should be manageable. We note that the geosynchronous orbit is a more stringent environment than the planned MMS orbit, so these rates would be lower for the actual MMS orbit.

It is not clear what the underlying physical mechanism(s) are, that are causing these destructive failures. There are two models in the literature, which could be useful in explaining some of our results. The first of these is by Brews et al., [2], who suggested that charge from the ion strike accumulates under the oxide by a process similar to funneling [3]. This accumulated charge creates a space-charge voltage, which adds to the applied voltage. The total field exceeds the breakdown threshold for the oxide, and actually blows a hole in the oxide (gate rupture). The angular dependence, that we have observed, falls out of this model very naturally. The voltage difference across the oxide is the same, at different angles. But the conducting path will be longer at high angles, which means the field will be lower, so gate rupture is less

likely at high angles. But this model does not account for percolation path forms all the way across the oxide. This model might explain why we see signs of accumulated damage being important. But it does not explain either the angular dependence or the temperature dependence in our results. Therefore, we conclude that there is no existing model that accounts for all our results.

VI. RECOMMENDATIONS

Our recommendation is to use these Samsung parts as flash memory on MMS. All flash memory has a bit upset rate that is outstanding, compared to typical volatile memories. The reason is that volatile memories lose information when ion strikes pull down voltages, but flash is designed to retain information, even with no voltage applied. Therefore flash is typically five or more orders of magnitude better than volatile memories in upset rate, and these Samsung parts are no exception. SEFIs are a more significant problem than bit errors in advanced flash memories, and, of course, destructive events are potential show stoppers. Both of these things are much less common for these Samsung parts than in, for example, the Micron parts tested earlier. On the Micron parts, there was a SEFI on nearly every shot, and we often lost data because the DUT basically shut down. It was actually hard to determine the upset rate because there were so many SEFIs. For the Samsung parts, SEFIs also occurred, but on a much smaller fraction of the shots. For the Micron parts, destructive events happened even in static mode at room temperature, at low LET, and at oblique angles. For the Samsung parts, destructive events also happened, but they typically required high temperature, high voltage, and just the right angle of incidence. Therefore, the risk of SEFIs and destructive failures appears to be much lower in these Samsung parts, than in others, but the risk is not zero. For this reason, it will be important to have a good strategy for managing these risks. We also note that the 2009 LDCs seem to have had better resistance to destructive effects than the 2008 LDCs, so using those parts as much as possible would seem to be a good plan. Therefore, we recommend using LDC 907 and 901 as much as possible, and not using LDC 840 if it can be avoided. In terms of resistance to destructive failures, LDCs 843 and 846 fell in the middle, and were about the same as each other.

VII. ACKNOWLEDGMENT

The authors wish to acknowledge the support of the MMS mission and the NEPP program for this work. We also wish to thank Martha O'Bryan for technical support in the preparation of the presentation materials for this paper.

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